Recitation 4

Simple Finite State Machines

# Introduction

In this laboratory assignment, you will be looking at different aspects of finite state machine design for a simple modulo-5 counter (it outputs: 0, 1, 2, 3, 4, 0, 1, 2, …). First, you will be creating Moore and Mealy state designs. Then, you will be using **behavioral** Verilog to create one version of the counter and test it.

# Collaboration Policy

You will be working in groups of 2-3. Groups are allowed to collaborate.

# Equipment

* Computer with Quartus Prime software

# Tasks

To receive credit for this lab, you must complete:

* Task 1: Design both a Moore and a Mealy style modulo-5 counter
* Task 2: Implement the modulo-5 counter in Quartus

You must complete all parts of this lab to receive credit. A TA must sign-off on the completion of each task. Ensure that the TA marks the completion of the tasks in Sakai.

# Grading

* Completing Recitation Tasks: 1 point (pass/fail)

Note: Items shown in red should be shown to a TA.

## 

## State Machine Design

In this part of the lab, design (state table and state transition diagram) **both a Moore and a Mealy design** for the modulo-5 counter. Make sure your state table and diagram are legible.

## Implementing the Counter in Verilog

In this part of the lab, you will be modifying a standard mod-8 synchronous counter (like the one in the lecture slides) to be a mod-5 counter (shown in Figure 1). You will need to implement either the Mealy or the Moore style counter in **behavioral** Verilog. The "events" we will count will be clock pulses (i.e., no separate input to enable counting). In the simulation, **have your counter trigger an output only when your count reaches "4"** (in the sequence 0-1-2-3-4-0-1-2-3-4...).

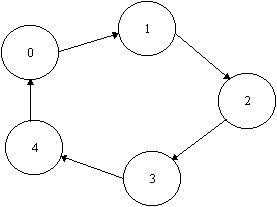


Figure 1. Modulo-5 Synchronous Counter State Diagram

You can use [this resource](https://verilogguide.readthedocs.io/en/latest/verilog/fsm.html) to help you implement FSMs using behavioral Verilog.

Note that we will need three flip-flops to implement this circuit. As there are 8 possible states of three flip-flops, 3 of the 8 will not be assigned. Consider what happens if the circuit should power up in one of the unassigned states (5, 6, 7). We want to ensure that even if this happens, the circuit will still behave as a Mod-5 counter immediately following the first clock pulse by including additional state transitions as shown in Figure 2.

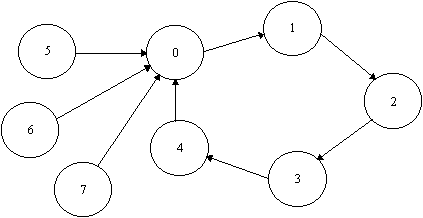


Figure 2. Complete Modulo-5 Synchronous Counter State Diagram

Simulate your designs using testbenches – a sample testbench is included in Figure 3. Show your Moore design, Mealy design, and testbench results to a TA once you are done.

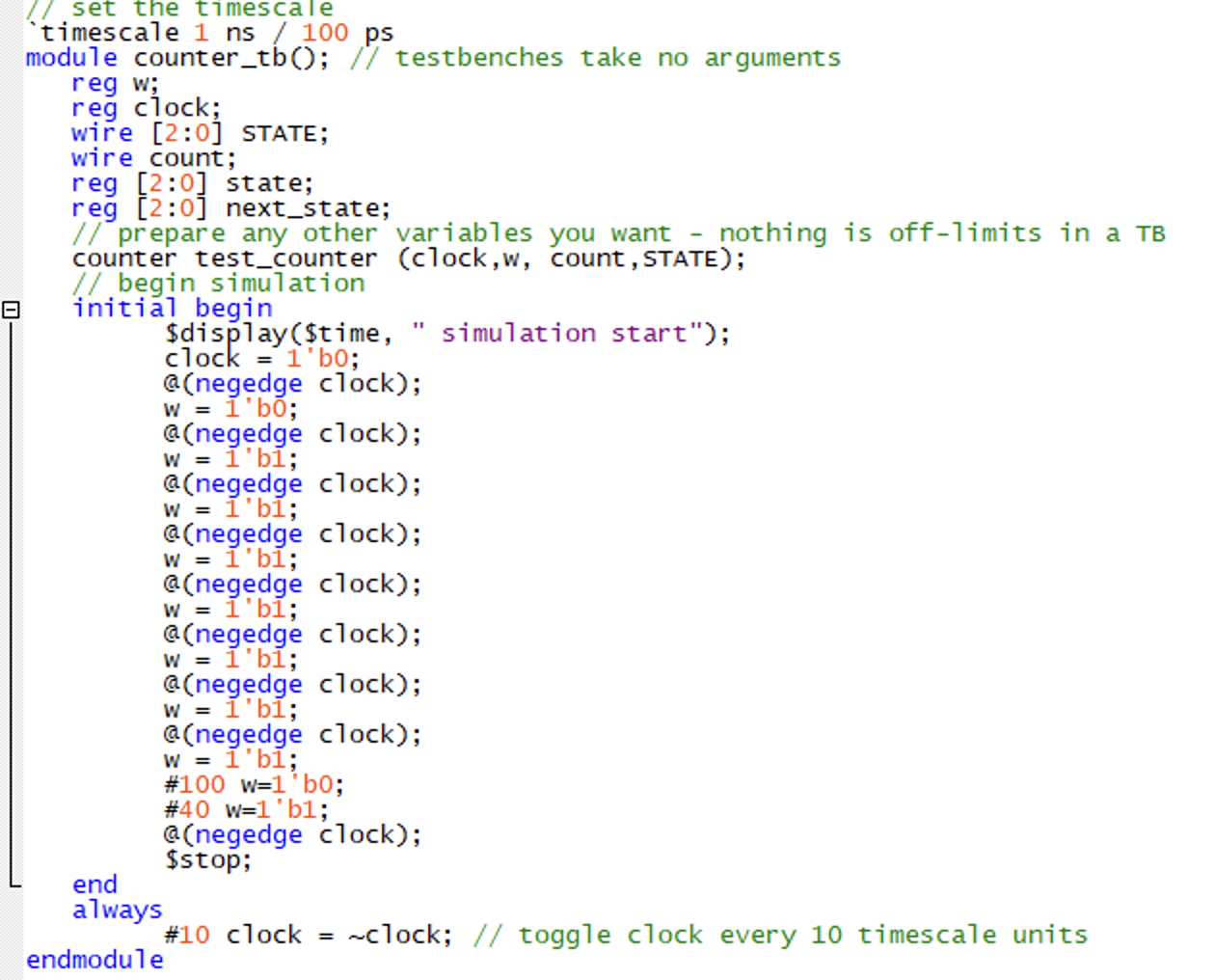


Figure 3. Sample testbench